



Powering FPGAs

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Abstract

Today, FPGAs are widely used universal components that can contain even complex systems on a single chip, thus enabling users to obtain an extremely short time-to-market. However, these versatile components have an urgent need for a favorable electrical current which allows them to make full use of their capabilities. One of the basic requirements of a power supply for FPGAs is to generate the necessary supply voltages in the best possible quality.

This article discusses FPGAs' power requirements and illustrates several general and specific paths to adequate power supply solutions.

Basic Concepts in Power Supply Design

The power supply design for an FPGA is one of the critical points in the design process, as the requirements are stringent and manifold, ranging from extremely low supply voltages like 0.9 for logic termination to 1.2 for core supply with high variation of current dissipation and low noise requirements. In most cases, but specifically for PLL supply, high efficiency is extremely important to minimize heat generation. Because the system is on a single chip, the complete system is designed to be compact and the power supply cannot tolerate an exception. Another requirement for the power supply is ease of use, as engineers with profound analog and power knowledge and experience are scarce.

What are the basic concepts?

Generally, the supply voltages needed for FPGAs are lower than those being fed to the board, which are typically at 5V or higher—one reason being the relationship of voltage, current and power. For a constant amount of power, the current and voltage are inversely proportional—as one increases, the other decreases. A high current requires bigger and more expensive connectors, wires and traces. FPGAs have historically used core voltages between 0.9V and 1.5V, but like everywhere else in the digital world, these voltage levels keep going down.

When low voltages need to be generated from higher voltage levels, there are two basic approaches: linear regulation or switched mode regulation, which uses the buck regulator architecture.

Linear regulators convert the input-output voltage difference to heat. They are easy to use (fig. 1a) and offer excellent noise performance. On the other hand, the efficiency becomes poor when the input-to-output voltage difference increases, as efficiency is roughly the output voltage to input voltage ratio. For example, when a 2.5V rail is generated from 5V then the efficiency is roughly 50%.

Nevertheless, there are cases when linear regulators outperform switch mode regulators not only for simplicity and low noise but also for efficiency. This is the case when the input to output voltage difference is low. Low dropout voltage, however, has led the world of electronics to use the term "low dropout

regulator” as a synonymous expression for a linear regulator. Semtech offers linear regulators that work from a supply voltage as low as 1.4V and dropout voltages as low as 250mV and low noise products as well.

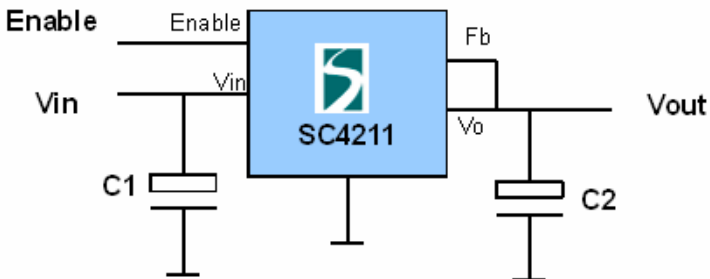


Fig. 1a: Linear regulators are easy to use

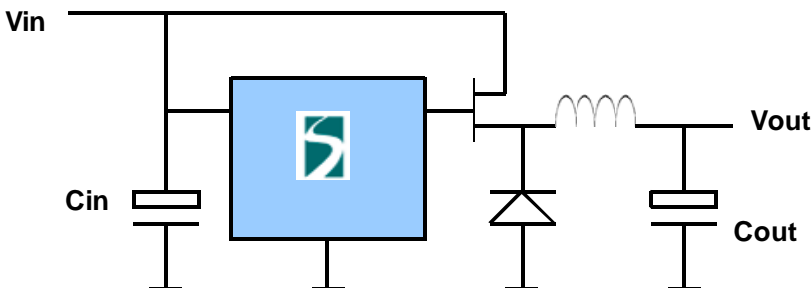


Fig. 1b: Buck regulators use a transistor switch to generate a lower voltage

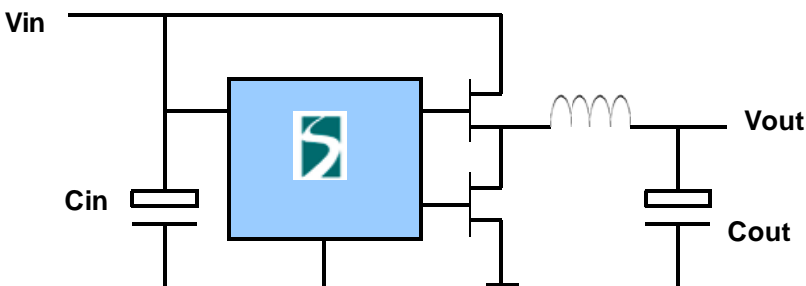


Fig. 1c: Synchronous Buck regulators use a transistor switch instead of the diode rectifier that yields higher efficiency

A switched regulator approach circumvents this poor efficiency problem. The general buck architecture (Fig. 1b) uses a transistor switch to direct the current to an inductor and the load. The current is allowed to flow for short periods of time, and the output voltage is directly proportional to the duty cycle, i.e. to the on/off ratio of the current flow. Power is mainly dissipated by the transistor, typically a MOSFET transistor with limited R_{DSon} , using the resistive components of the inductor and the output capacitor, while the energy is used to put the MOSFET into and out of conduction mode. Hence the converter's efficiency is less dependent on the input to output voltage ratio than on the choice of components and conversion frequency.

Low conversion frequency usually yields lower conversion loss at the cost of bulky inductors and capacitors and need for more board space. It is now common to use conversion frequencies in the lower Megahertz range at an efficiency level of 85-95 %. Particularly when output voltages below 2V are generated, the forward voltage of the rectifier diode in Fig. 1b adds considerably to the conversion losses. To avoid this, the synchronous buck converter (Fig. 1c) uses another MOSFET instead of the rectifier diode to ensure lower voltage drop. For both architectures Semtech offers controllers and regulators with integrated MOSFETs that simplify the design and minimize board space.

Calculating FPGA Power Consumption

In order to estimate the power supply requirements, the FPGA manufacturer provides a means for calculating the current consumption for each supply voltage. Sometimes this is done with simple EXCEL spreadsheets or, as is the case for Lattice Semiconductor, by use of the Power Calculator software.

This tool enables the designer to estimate the current consumption in an early design phase—even before the logic design as such has been started. The only inputs necessary are the number of look-up-tables (LUTs) used, the number of registers, memory, PLLs and I/Os, together with the associated clock frequency and activity factor. The Power Calculator tool calculates the current consumption for each individual supply voltage, dependent on ambient resp. chip temperature. Even a rough estimation of the thermal environment is enough for the calculations (Fig. 2). It is possible to select for board size, heat sink and airflow.

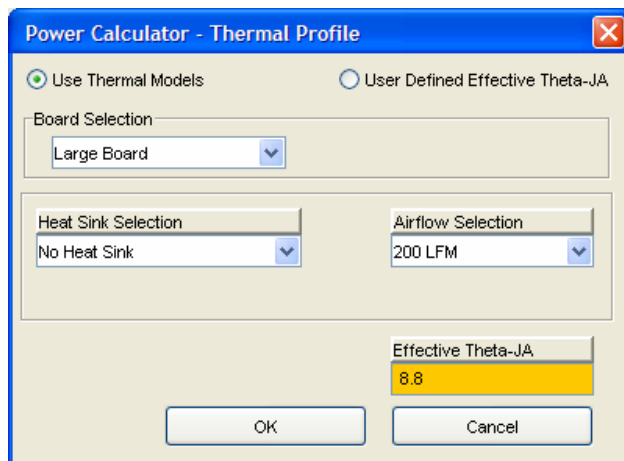


Fig. 2: Setting the ambient conditions

The graph in fig. 3 shows the relationship of power dissipation and ambient temperature. This example is based on the ECP2M-20 in BGA256 package. The design uses 16 k LUTs and 10 k registers, 40 memory blocks, 6 sysDSP blocks, 4PLLs, 2 DLLs and 4 SERDES channels. The I/Os use 40 LVDS outputs, 40 CMOS outputs with a driver strength of 4 mA and a bidirectional 32 bit bus in LVCMOS3.3. The clock frequency is set to 125 MHz, and the activity factor (AF) is 20 %, which is a good value for “typical” applications.

It is an important point to check the die temperature (junction temperature) at the given circumstance, though, as it must not exceed the value specified in the data sheet. If this danger is still a viable possibility, it is necessary to work on the design parameters on the heat sink or the amount of airflow.

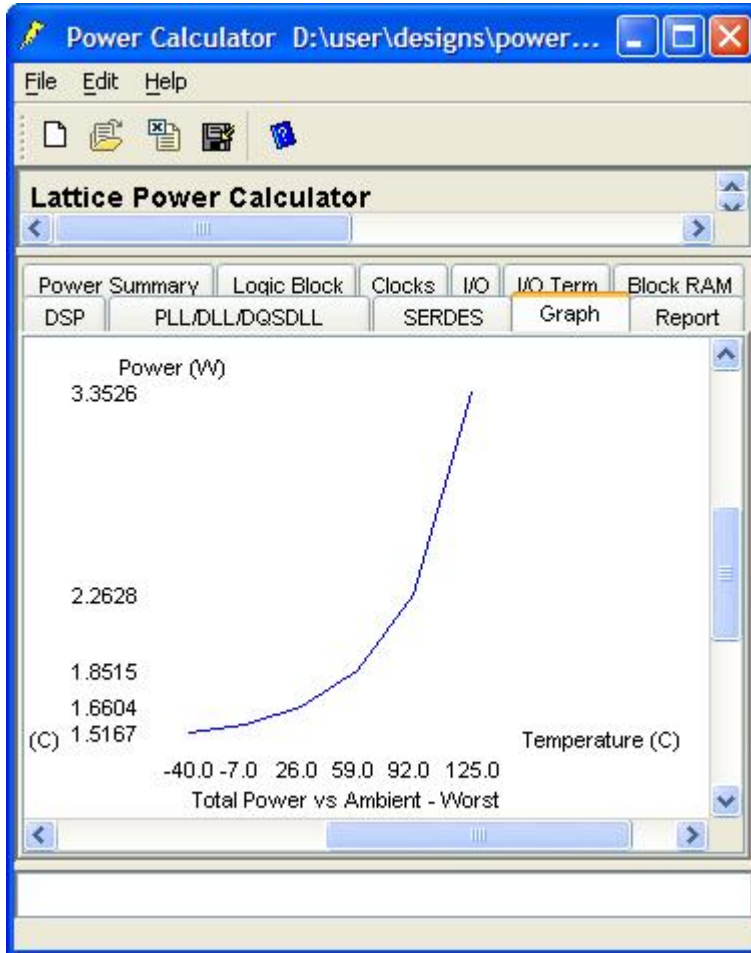


Fig. 3: Power dissipation as a function of ambient temperature

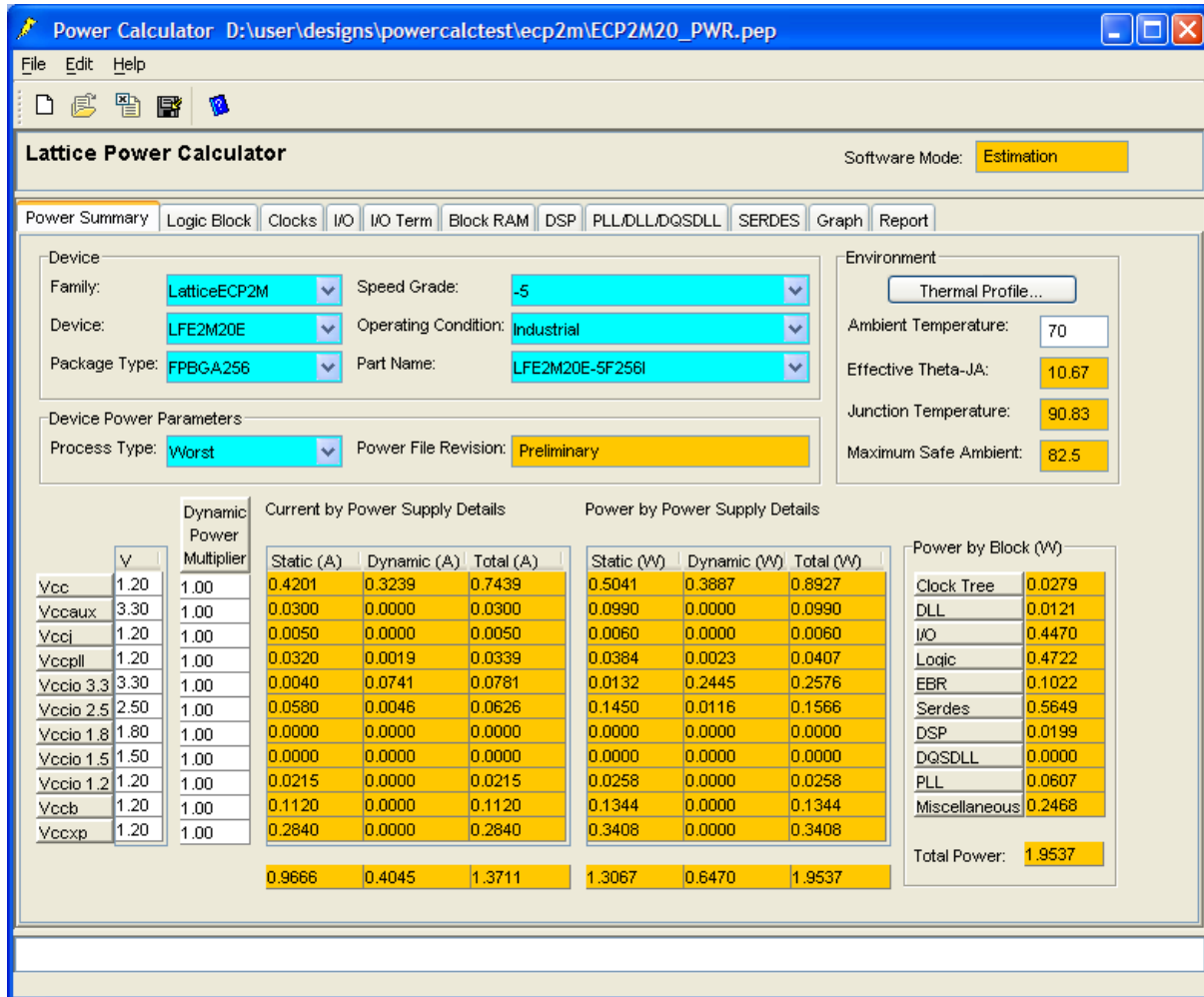


Fig. 4: Current/power details per supply voltage rail

The overview in Fig. 4 demonstrates that the biggest part of the power dissipation is static.

Once a design has been implemented using the ispLEVER software in a later stage, the design data can be loaded into the Power Calculator and measured more accurately.

Supplying an FPGA from the XP2-Family

The FPGAs from Lattice Semiconductor's XP2 family are fully featured with Flash boot memory on board, using an industry-standard look-up-table-architecture. The LUTs can also be configured to function as tiles of distributed memory. The complete family comprises complexities from 5,000 to 40,000 look-up-tables and an additional 166 to 885 kbits of embedded memory with sysDSP blocks that are capable of adding, subtracting, multiplying and accumulating. They allow simple and efficient implementation of FIR and IIR structures as well as complex math.

The family supports manifold logic standards like LVCMOS, PCI, LVTTTL, LVDS, SSTL and HSTL. Additionally, from a power supply designer's standpoint, XP2 is attractive. In the simplest application case, only two supply voltages are necessary to run the FPGA, and there is no need to sequence the supply voltages.

In detail, these supply voltages are needed:

- a Core Voltage of nom. 1.2 V
- an Auxiliary Supply Voltage VCC_{aux} of nom. 3.3 V
- a PLL supply voltage VCC_{pll} of nom. 3.3 V
- I/O-supply voltages VCC_{io} between 1.2 V and 3.3 V according to the I/O standards used and
- a JTAG- voltage VCC_j between 1.2 V and 3.3 V.

An application example with XP2-12 as a control element using 3.3 V I/Os and a few high speed LVDS I/Os. These need an additional supply voltage of 2.5V.

Based on the Power Calculator, the requirements for the individual power supplies are as follows:

For the FPGA Core: 1.2 V, max. 700 mA

For VCC_{aux} , VCC_j and the CMOS-I/Os max. 300 mA and

For the LVDS- VCC_{io} max. 50 mA.

The available supply voltage is 4.5 – 5.5 V.

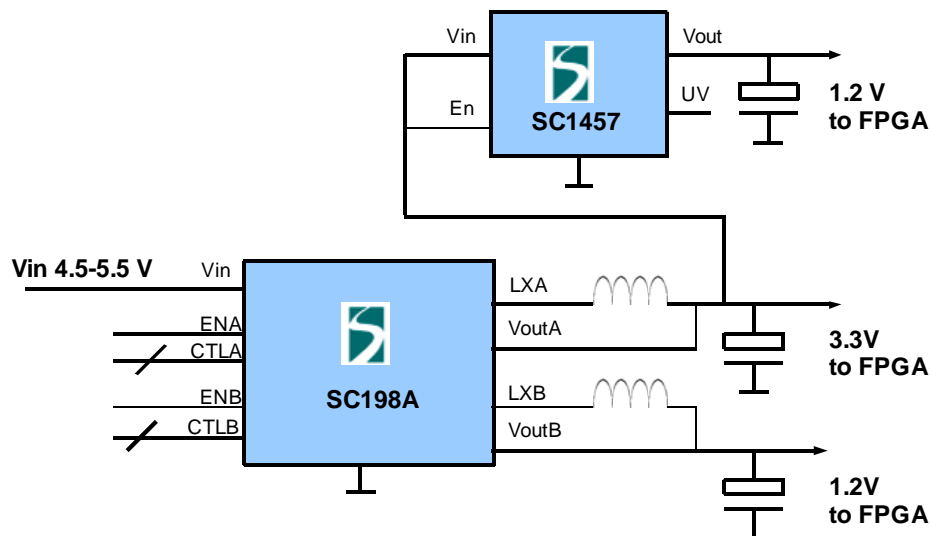


Fig. 5: The power supply for the XP2-FPGA consists of a dual buck converter SC198A and a Low-Dropout-Regulator SC1457.

A dual buck regulator SC198A was used to generate 3.3 V and 1.2 V from 4.5 – 5.5 V; a linear regulator SC1457 is used to drop the 3.3 V rail to 2.5 V.

The SC198A is a fully integrated dual buck converter with the top and bottom MOSFET transistors integrated—thus needing few external parts. Both output voltages can be individually programmed through a set of voltage selection pins, and the output current can be as high as 800 mA for each output.

The conversion frequency is internally set to 1 MHz and can be synchronized to a master frequency, which would need to be supplied externally. Both outputs can be enabled individually, allowing sequencing without additional efforts.

In low load situations, a power save mode can be activated to retain superior efficiency. The compact MLPQ20 package, combined with high integration, offers a solution with great power density.

SC1457 is a low drop regulator that can supply a maximum output current of 150 mA at a dropout voltage of 150 mV. It features an enable input for simple sequencing and an undervoltage output in a tiny SOT23 package.

Supplying a PCI-Express board with ECP2/M

The ECP2/M-Family from Lattice Semiconductor offers up to 95,000 look up tables in a low cost FPGA architecture, along with sysDSP-Blocks, 5 Mbits of embedded memory, bitstream encryption and I/Os that work at speeds up to 800 Mbps. In addition, there are up to 16 SERDES-channels that can transfer data at a speed up to 3.125 Gbps. Using the combination of these capabilities, it is possible to implement a complete PCI Express interface with a large amount of additional functionality. By adding a DDR2 memory module, it is possible to generate an extremely compact PCI Express system for a wide variety of applications.

For the FPGA, these supply rails are needed:

- a core voltage VCC nom. 1.2 V
- an auxiliary supply voltage VCCaux nom. 3.3 V
- a PLL supply voltage VCCpll nom. 1.2 V
- I/O supply voltages VCCio ranging from 1.2 V to 3.3 V depending on I/O standards and
- a JTAG voltage VCCj between 1.2 V and 3.3 V.

For the interface from the FPGA to the DDR2 memory module, SSTL1.8 is the appropriate I/O standard, which requires approximately 100 I/Os to be supplied from 1.8 V.

For the SERDES blocks, these additional voltages are needed:

- one supply VCCib und VCCob of 1.2 V or 1.5 V nom. For input and output buffers
- one supply for receivers and transmitters , VCCrx und VCCtx, nom. 1.2 V and
- SERDES-PLL voltage Vccp nom. 1.2 V.

The DDR2 memory module requires these voltages:

- supply voltage VDD nom. 1.8V,
- termination voltage VDD/2, nom. 0.9 V and
- VDDspd for the serial EEPROM, 1.7V to 3.6V.

The calculation of the power dissipation reveals these supply current requirements:

3.3 V/ 0.5 A

1.8 V/ 1.5 A

1.2 V/ 2 A

0.9 V/0.5 A.

The PCI Express standard specifies supply voltage rails of 12 V at a max current—5.5 A and of 3.3 V rail at a max current of 3.0 A over the PCIe system connector. This means that the 3.3 V rail is not capable of supplying the required power to the board, and it is probably a better solution to use the 12 V rail to generate the required voltage rails. It is good practice to generate an intermediate voltage rail such as a 3.3 V, which is needed in the system anyway. This can be accomplished by using a buck controller like SC4612 (Fig. 6), which leverages external MOSFETs and can be optimized for best efficiency or, as an alternative, with the SC417. This new component contains both the controller and the MOSFETs in a 5x5 mm MLPQ package and allows extremely compact power supply solutions.

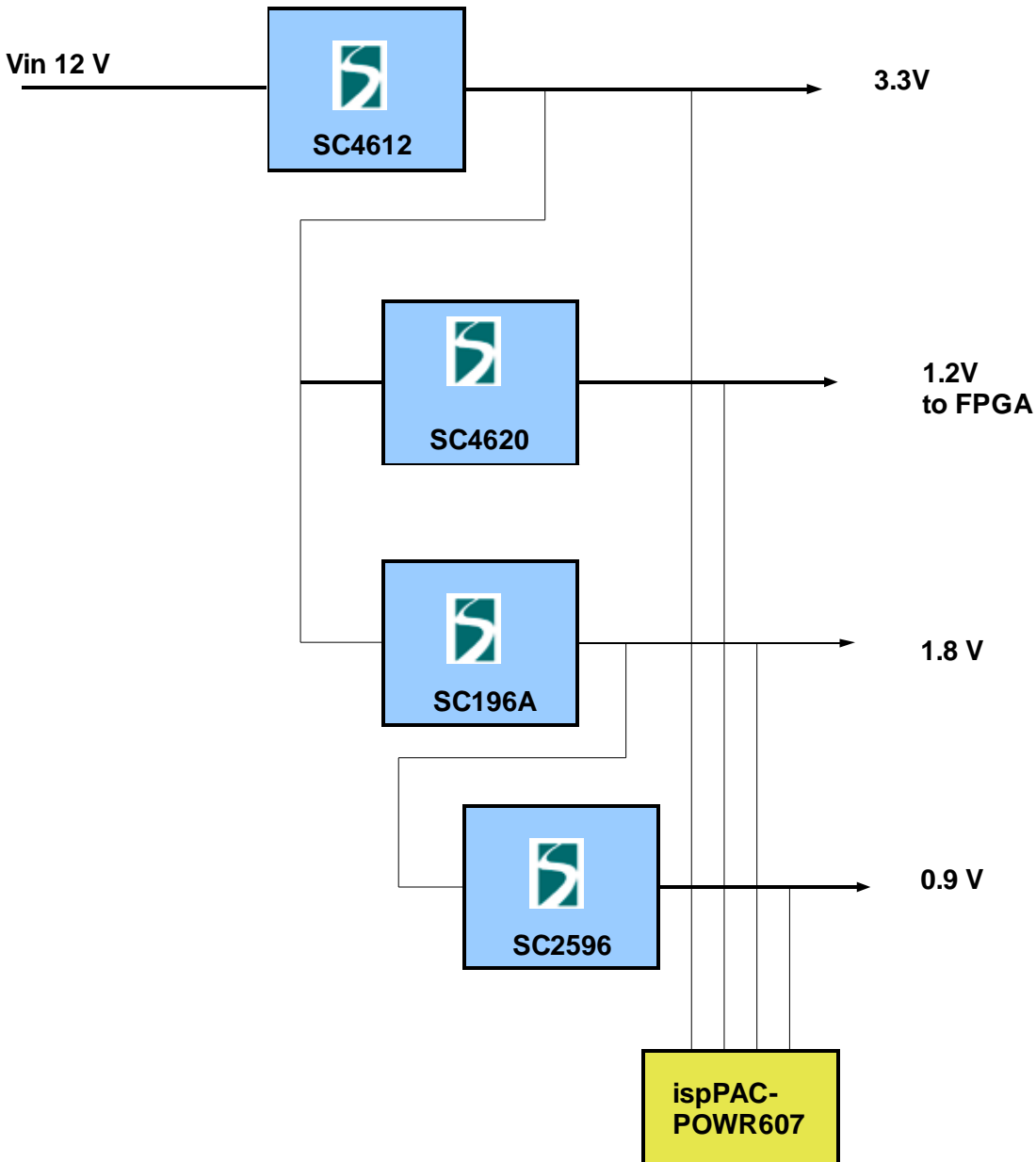


Fig. 6: Example of a power supply setup for PCIe board

According to Fig. 6, the intermediate voltage of 3.3V can then be used by “low voltage” buck converters to generate the core voltage of 1.2 and the memory supply voltage of 1.8. These voltage rails can be monitored by a programmable power management chip like the ispPAC607 from Lattice Semiconductor.

Table 1 summarizes Semtech’s portfolio of highly integrated buck converters.

Part Number	Product Description	Vin Min	Vin Max	Iout Max	Vout Min	Packages
SC4624 SC4624A	Low Input Voltage, High Efficiency, 4A Integrated FET Synchronous Step down DC/DC Regulator	2.3	5.5	4	0.5	SO-16 EDP,MLPQ-20
SC4620	Low Input Voltage, High Efficiency, 2.5A Integrated FET Synchronous Step down DC/DC Regulator	2.3	5.5	2.5	0.5	4mm x 4mm MLPQ-20
SC196 SC196A	1.5A Synchronous Buck Converter with Integrated Power Devices	2.7	5.5	1.5	1.0	MLPD-10
SC194A SC194B SC198 SC198A	Selectable 3.6V/3.3V/3.0V/2.5V 1A Synchronous Buck Converter Dual DC-DC Buck Converter with High Current Capability	2.7	5.5	1	1.0	MLP-10 MLPQ-20
SC192	Synchronous Buck Converter with Integrated Power Devices	2.7	5.5	0.7	0.8	MLP-10
SC191	Low Supply Ripple Synchronous Buck Conversion Regulator	2.7	5.5	0.33	1.2	MLP-8
SC190	Synchronous Buck Converter with Programmable Output	2.7	7	0.3	1.4	MLP-10

Table 1: Integrated Buck Converters form Semtech

The termination voltage for the data lines from the FPGA to the DDR2 module is generated by a special linear regulator, the SC2596. This device does not regulate for a constant output voltage, but it follows the memory module input voltage and is capable of sourcing and sinking current.

Lots of design support

Putting together the power supply architecture for your FPGA project is an important starting point. For schematics and layout, there is extensive design support from Semtech, like documentation on the Website www.semtech.com, evaluation boards, free samples and design and layout reviews.



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